



59C11

1K 5.0V Microwire[®] Serial EEPROM

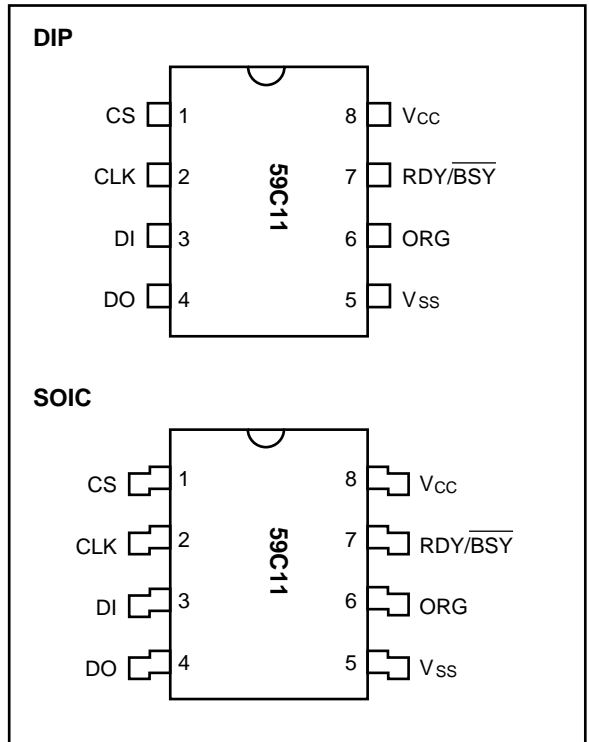
FEATURES

- Low power CMOS technology
- Pin selectable memory organization
 - 128 x 8 or 64 x 16 bit organization
- Single 5V only operation
- Self timed WRITE, ERAL and WRAL cycles
- Automatic erase before WRITE
- RDY/ $\overline{\text{BSY}}$ status information during WRITE
- Power on/off data protection circuitry
- **1,000,000 ERASE/WRITE cycles guaranteed**
- Data Retention > 200 Years
- 8-pin DIP or SOIC package
- Temperature ranges supported
 - Commercial (C): 0°C to +70°C
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

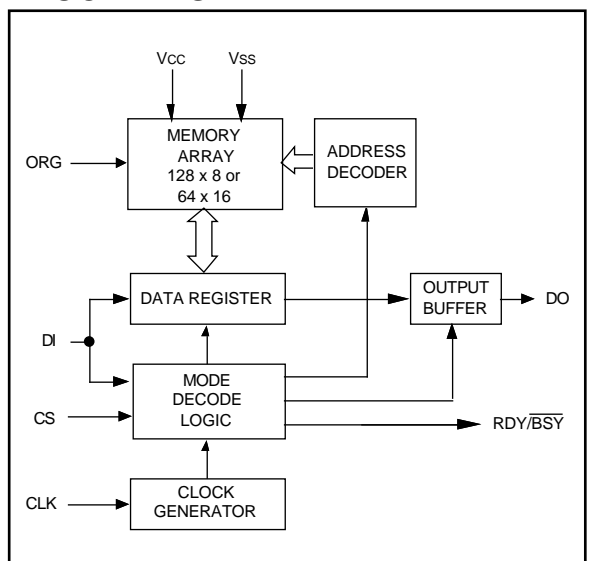
DESCRIPTION

The Microchip Technology Inc. 59C11 is a 1K bit Electrically Erasable PROM. The device is configured as 128 x 8 or 64 x 16, selectable externally by means of the control pin ORG. Advanced CMOS technology makes this device ideal for low power nonvolatile memory applications. The 59C11 is available in the standard 8-pin DIP and a surface mount SOIC package.

PACKAGE TYPES



BLOCK DIAGRAM



Microwire is a registered trademark of National Semiconductor Incorporated.

59C11

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}.....7.0V
 All inputs and outputs w.r.t. V_{SS} -0.6V to V_{CC} +1.0V
 Storage temperature -65°C to +150°C
 Ambient temperature with power applied..... -65°C to +125°C
 Soldering temperature of leads (10 seconds) +300°C
 ESD protection on all pins..... 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
CS	Chip Select
CLK	Serial Clock
DI	Data In
DO	Data Out
V _{SS}	Ground
ORG	Memory Array Organization
RDY/ $\overline{\text{BSY}}$	Ready/Busy Status
V _{CC}	+5V Power SUPPLY

TABLE 1-2: DC CHARACTERISTICS

V _{CC} = +5.0V (±10%)					
Commercial (C): T _{amb} = 0°C to 70°C					
Industrial (I): T _{amb} = -40°C to +85°C					
Automotive (E): T _{amb} = -40°C to 125°C					
Parameter	Symbol	Min	Max	Units	Conditions
V _{CC} detector threshold	V _{TH}	2.8	4.5	V	
High level input voltage	V _{IH}	2.0	V _{CC} +1	V	
Low level input voltage	V _{IL}	-0.3	0.8	V	
High level output voltage	V _{OH}	2.4	—	V	I _{OH} = -400 μA
Low level output voltage	V _{OL}	—	0.4	V	I _{OL} = 3.2 mA
Input leakage current	I _{LI}	—	10	μA	V _{IN} = 0V to V _{CC} (Note 1)
Output leakage current	I _{LO}	—	10	μA	V _{OUT} = 0V to V _{CC} (Note 1)
Pin capacitance (all inputs/outputs)	C _{IN} , C _{OUT}	—	7	pF	V _{IN} /V _{OUT} = 0V (Note 2) T _{amb} = 25°C, f = 1 MHz
Operating current (all modes)	I _{CC} write	—	4	mA	FCLK = 1 MHz, V _{CC} = 5.5V
Standby current	I _{CCS}	—	100	μA	CS = 0V, V _{CC} = 5.5V

Note 1: Internal resistor pull-up at Pin 6. Active output at Pin 7.
 Note 2: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: SYNCHRONOUS DATA TIMING

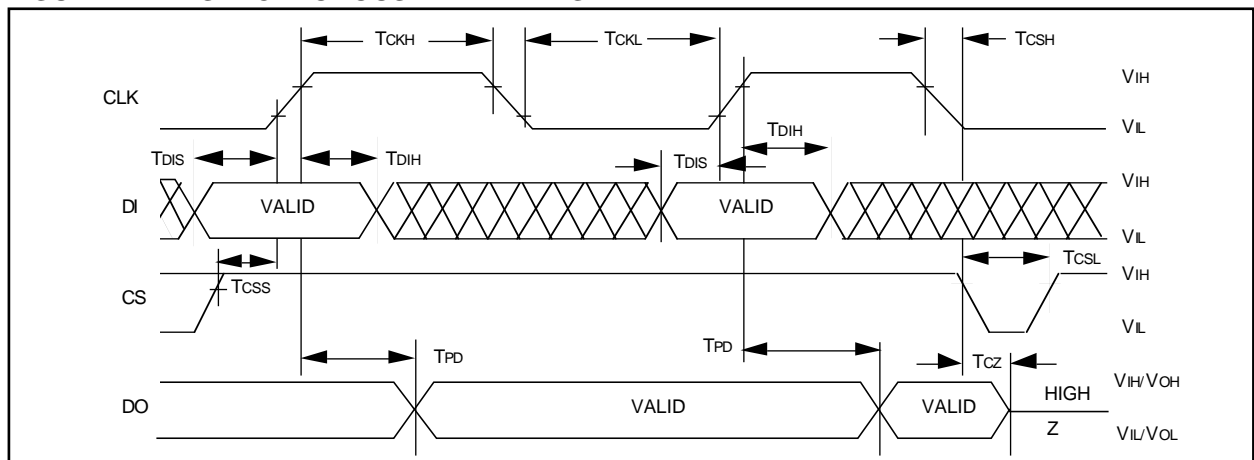


TABLE 1-3: AC CHARACTERISTICS

Parameter	Symbol	Min	Max	Units	Conditions
Clock frequency	FCLK		1	MHz	
Clock high time	TCKH	500	—	ns	
Clock low time	TCKL	500	—	ns	
Chip select setup time	TCSS	50	—	ns	
Chip select hold time	TCSH	0	—	ns	
Chip select low time	TCS	100	—	ns	
Data input setup time	TDIS	100	—	ns	
Data input hold time	TDIH	100	—	ns	
Data output delay time	TPD	—	400	ns	CL = 100 pF
Data output disable time (from CS = low)	TCZ	0	100	ns	CL = 100 pF
Data output disable time (from last clock)	TDDZ	0	400	ns	CL = 100 pF
RDY/ $\overline{\text{BSY}}$ delay time	TRBD	—	400	ns	
Program cycle time (Auto Erase and Write)	Twc	—	1 15	ms ms	for 8-bit mode for ERAL and WRAL in 8/16-bit modes
Endurance	—	1M	—	cycles	25°C, Vcc = 5.0V, Block Mode (Note 1)

Note 1: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

TABLE 1-4: INSTRUCTION SET

6 X 16 MODE, ORG = 1						
Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A5 A4 A3 A2 A1 A0	—	D15-D0	27
WRITE	1	X 1 X X	A5 A4 A3 A2 A1 A0	D15-D0	High-Z	27
EWEN	1	0 0 1 1	X X X X X X	—	High-Z	11
EWDS	1	0 0 0 0	X X X X X X	—	High-Z	11
ERAL	1	0 0 1 0	X X X X X X	—	High-Z	11
WRAL	1	0 0 0 1	X X X X X X	D15-D0	High-Z	27
128 X 8 MODE, ORG = 0						
Instruction	Start Bit	Opcode	Address	Data In	Data Out	Number of Req. CLK Cycles
READ	1	1 0 X X	A6 A5 A4 A3 A2 A1 A0	—	D7-D0	20
WRITE	1	X 1 X X	A6 A5 A4 A3 A2 A1 A0	D7-D0	High-Z	20
EWEN	1	0 0 1 1	X X X X X X X	—	High-Z	12
EWDS	1	0 0 0 0	X X X X X X X	—	High-Z	12
ERAL	1	0 0 1 0	X X X X X X X	—	High-Z	12
WRAL	1	0 0 0 1	X X X X X X X	D7-D0	High-Z	20

59C11

2.0 FUNCTIONAL DESCRIPTION

2.1 START Condition

The START bit is detected by the device if CS and DI are both High with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition) without resulting in any device operation (READ, WRITE, EWEN, EWDS, ERAL, and WRAL). As soon as CS is HIGH, the device is no longer in the standby mode.

An instruction following a START condition will only be executed if the required amount of opcode, address and data bits for any particular instruction is clocked in.

After execution of an instruction (i.e. clock in or out of the last required address or data bit) CLK and DI become don't care bits until a new start condition is detected.

Note: CS must go LOW between consecutive instructions.

2.2 DI/DO Pins

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the READ operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin.

2.3 Data Protection

During power-up, all modes of operation are inhibited until VCC has reached a level of 2.8 V. During power-down, the source data protection circuitry acts to inhibit all modes when VCC has fallen below 2.8 V.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

After power-up, the device is automatically in the EWDS mode. Therefore, EWEN instruction must be performed before any WRITE, ERAL or WRAL instruction can be executed. After programming is completed, the EWDS instruction offers added protection against unintended data changes.

2.4 READ Mode

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy bit (logical 0) precedes the 8- or 16-bit output string. The output data changes during the high state of the system clock (CLK). The dummy bit is output TPD after the positive edge of CLK, which was used to clock in the last address bit (A0). Therefore, care must be taken if DI and DO are connected together as a bus contention will occur for one clock cycle if A0 is a one.

DO will go into HIGH-Z mode with the positive edge of the next CLK cycle. This follows the output of the last data bit D0 or the negative edge of CS, whichever occurs first. D0 remains stable between CLK cycles for an unlimited time as long as CS stays HIGH.

The most significant data bit (D15 or D7) is always output first, followed by the lower significant bits (D14 - D0 or D6 - D0).

2.5 WRITE

The WRITE instruction is followed by 8 or 16 bits of data which are written into the specified address. The most significant data bit (D15 or D7) has to be clocked in first followed by the lower significant data bits (D14 - D0 or D6 - D0). If a WRITE instruction is recognized by the device and all data bits have been clocked in, the device performs an automatic erase cycle on the specified address before the data are written. The WRITE cycle is completely self timed and commences automatically after the rising edge of the CLK signal for the last data bit (D0).

The WRITE cycle takes 1 ms maximum for 8-bit mode and 2 ms maximum for 16-bit mode.

2.6 Erase/Write Enable and Disable (EWEN, EWDS)

The device is automatically in the ERASE/WRITE Disable mode (EWDS) after power-up. Therefore, EWEN instruction has to be performed before any WRITE, ERAL, or WRAL instruction is executed by the device. For added data protection, the device should be put in the ERASE/WRITE Disable mode (EWDS) after programming operations are completed.

2.7 ERASE All (ERAL)

The entire chip will be erased to logical "1s" if this instruction is received by the device and it is in the EWEN mode. The ERAL cycle is completely self-timed and commences after the rising edge of the CLK signal for the last dummy address bit. ERAL takes 15 ms maximum.

2.8 WRITE All (WRAL)

The entire chip will be written with the data specified in that command. The WRAL cycle is completely self-timed and commences after the last data bit (D0) has been clocked in. WRAL takes 15 ms maximum.

Note: The WRAL does not include an automatic ERASE cycle for the chip. Therefore, the WRAL instruction must be preceded by an ERAL instruction and the chip must be in the EWEN status in both cases. The WRAL instruction is used for testing and/or device initialization.

FIGURE 2-1: READ MODE

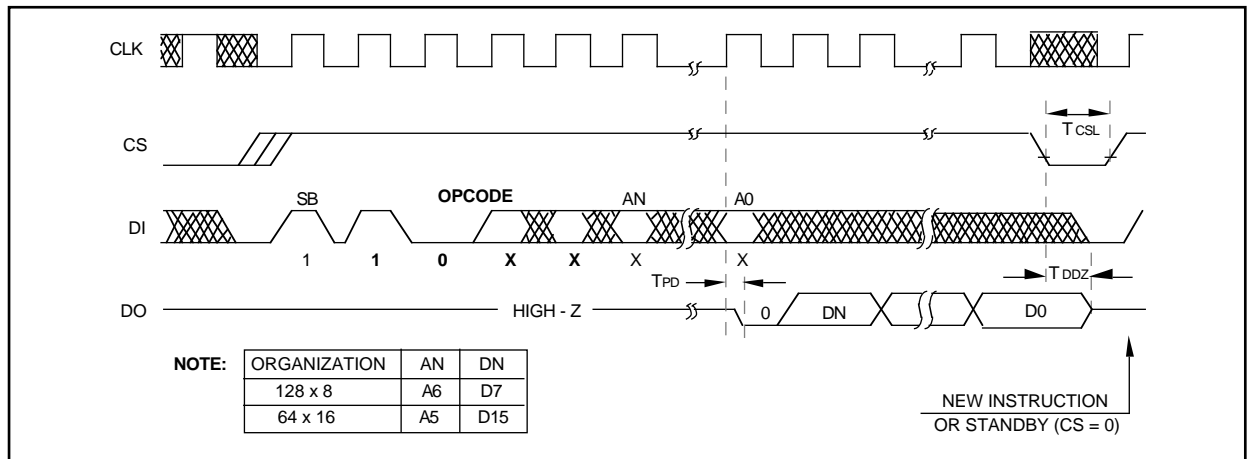
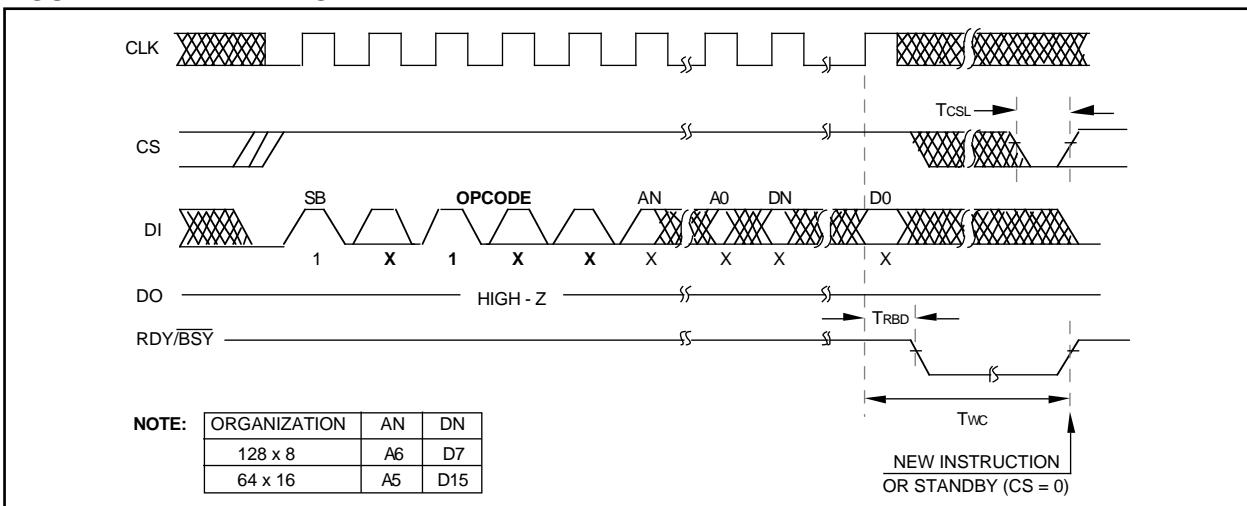


FIGURE 2-2: WRITE MODE



59C11

FIGURE 2-3: ERASE/WRITE ENABLE AND DISABLE

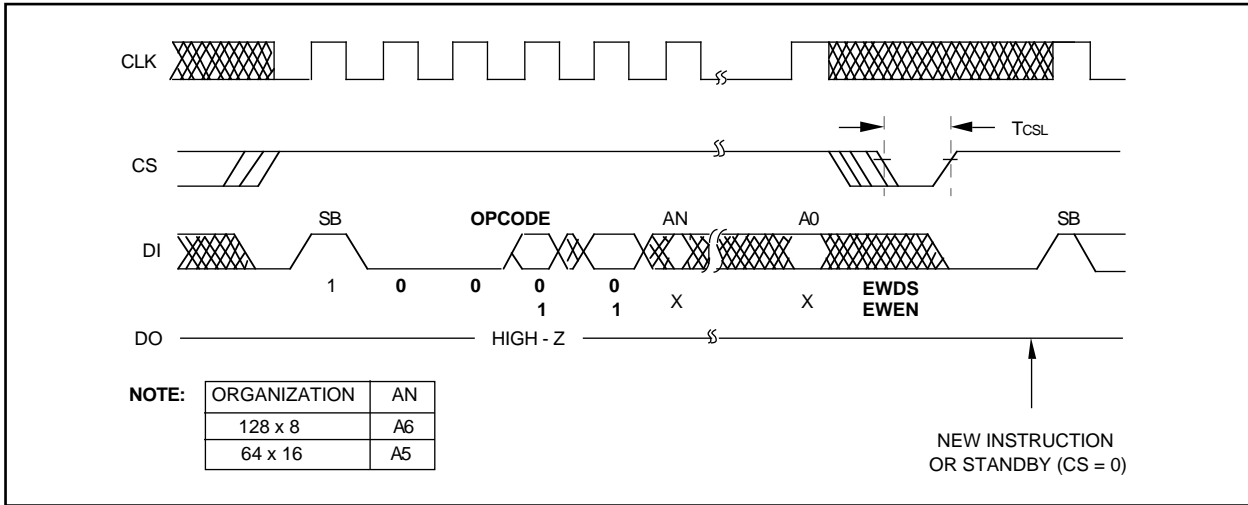


FIGURE 2-4: ERASE ALL (ERAL)

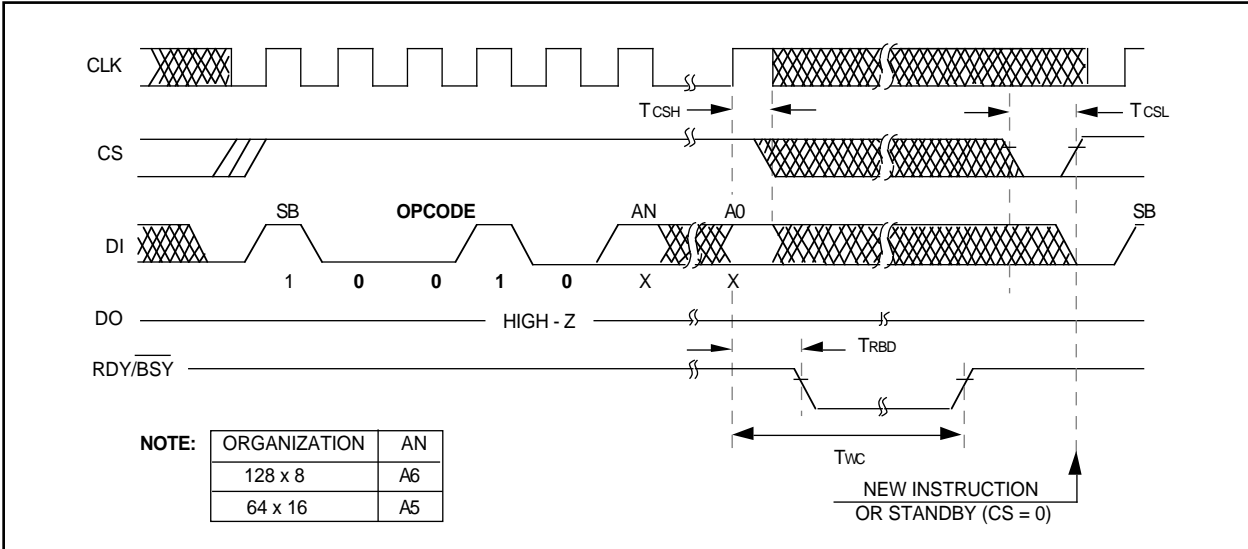
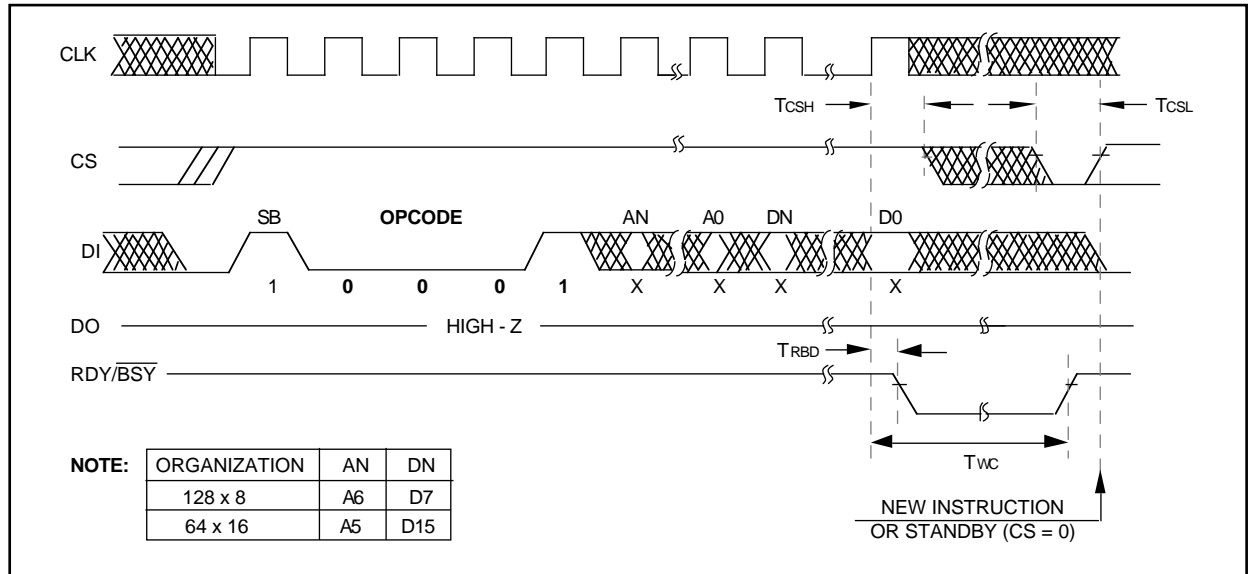


FIGURE 2-5: WRITE ALL



3.0 PIN DESCRIPTION

3.1 Chip Select (CS)

A HIGH level selects the device. A LOW level deselects the device and forces it into standby mode. However, a WRITE cycle which is already initiated and/or in progress will be completed, regardless of the CS input signal. If CS is brought LOW during a WRITE cycle, the device will go into standby mode as soon as the WRITE cycle is completed.

CS must be LOW for 100 ns (T_{CSL}) minimum between consecutive instructions. If CS is LOW, the internal control logic is held in a RESET status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 59C11. Opcode, address, and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at HIGH or LOW level) and can be continued anytime (with respect to clock high time (T_{CKH}) and clock low time (T_{CKL})). This gives freedom in preparing opcode, address and data for the controlling master.

CLK is a "Don't Care" if CS is LOW (device deselected). If CS is HIGH, but a START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto erase/write) cycle.

After detection of a START condition the specified number of clock cycles (respectively LOW to HIGH transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address, and data bits before an instruction is executed (see instruction set truth table). When that limit has been reached, CLK and DI become "Don't Care" inputs until CS is brought LOW for at least chip select low time (T_{CSL}) and brought HIGH again and a WRITE cycle (if any) is completed.

3.3 Data In (DI)

Data In is used to clock in START bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out is used in the READ mode to output data synchronously with the CLK input (T_{PD} after the positive edge of CLK). This output is in HIGH-Z mode except if data is clocked out as a result of a READ instruction.

DI and DO can be connected together to perform a 3-wire interface (CS, CLK, DI/DO).

Care must be taken with the leading dummy zero which is output after a READ command has been detected. Also, the controlling device must not drive the DI/DO bus during WRITE cycles.

3.5 Organization (ORG)

This input selects the memory array organization. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground, the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization. In applications subject to electrical noise, it is recommended that this pin not be left floating, but tied either high or low.

3.6 Ready/Busy (RDY/BSY)

Pin 7 provides RDY/\overline{BSY} status information. RDY/BSY is low if the device is performing a WRITE, ERAL, or WRAL operation. When it is HIGH the internal, self-timed WRITE, ERAL or WRAL operation has been completed and the device is ready to receive a new instruction.

59C11

NOTES:

NOTES:

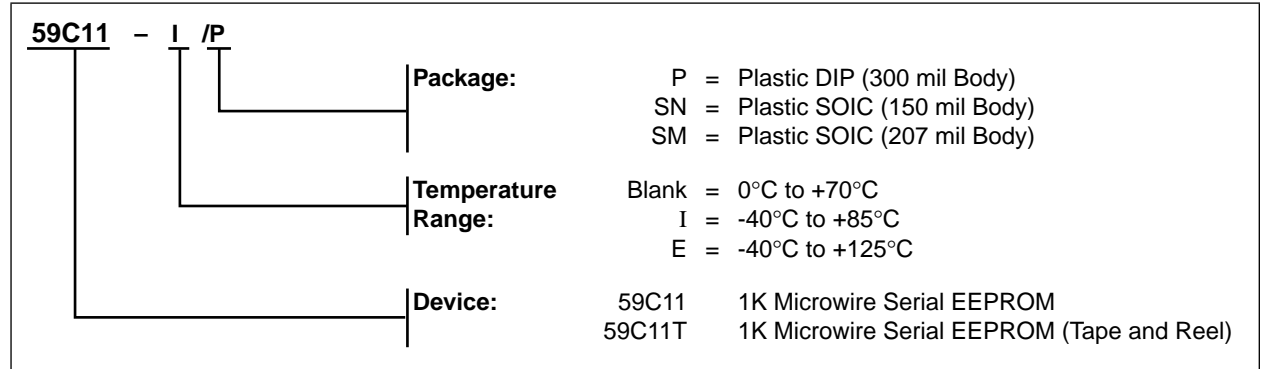
59C11

NOTES:

59C11

59C11 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.



WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office

Microchip Technology Inc.
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 602 786-7200 Fax: 602 786-7277
Technical Support: 602 786-7627
Web: <http://www.microchip.com>

Atlanta

Microchip Technology Inc.
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770 640-0034 Fax: 770 640-0307

Boston

Microchip Technology Inc.
5 Mount Royal Avenue
Marlborough, MA 01752
Tel: 508 480-9990 Fax: 508 480-8575

Chicago

Microchip Technology Inc.
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 708 285-0071 Fax: 708 285-0075

Dallas

Microchip Technology Inc.
14651 Dallas Parkway, Suite 816
Dallas, TX 75240-8809
Tel: 972 991-7177 Fax: 972 991-8588

Dayton

Microchip Technology Inc.
Suite 150
Two Prestige Place
Miamisburg, OH 45342
Tel: 513 291-1654 Fax: 513 291-9175

Los Angeles

Microchip Technology Inc.
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 714 263-1888 Fax: 714 263-1338

New York

Microchip Technmgy Inc.
150 Motor Parkway, Suite 416
Hauppauge, NY 11788
Tel: 516 273-5305 Fax: 516 273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408 436-7950 Fax: 408 436-7955

Toronto

Microchip Technology Inc.
5925 Airport Road, Suite 200
Mississauga, Ontario L4V 1W1, Canada
Tel: 905 405-6279 Fax: 905 405-6253

ASIA/PACIFIC

China

Microchip Technology
Unit 406 of Shanghai Golden Bridge Bldg.
2077 Yan'an Road West, Hongjiao District
Shanghai, Peoples Republic of China
Tel: 86 21 6275 5700
Fax: 011 86 21 6275 5060

Hong Kong

Microchip Technology
RM 3801B, Tower Two
Metroplaza
223 Hing Fong Road
Kwai Fong, N.T. Hong Kong
Tel: 852 2 401 1200 Fax: 852 2 401 3431

India

Microchip Technology
No. 6, Legacy, Convent Road
Bangalore 560 025 India
Tel: 91 80 526 3148 Fax: 91 80 559 9840

Korea

Microchip Technology
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku,
Seoul, Korea
Tel: 82 2 554 7200 Fax: 82 2 558 5934

Singapore

Microchip Technology
200 Middle Road
#10-03 Prime Centre
Singapore 188980
Tel: 65 334 8870 Fax: 65 334 8850

Taiwan, R.O.C

Microchip Technology
10F-1C 207
Tung Hua North Road
Taipei, Taiwan, ROC
Tel: 886 2 717 7175 Fax: 886 2 545 0139

EUROPE

United Kingdom

Arizona Microchip Technology Ltd.
Unit 6, The Courtyard
Meadow Bank, Furlong Road
Bourne End, Buckinghamshire SL8 5AJ
Tel: 44 1628 850303 Fax: 44 1628 850178

France

Arizona Microchip Technology SARL
Zone Industrielle de la Bonde
2 Rue du Buisson aux Fraises
91300 Massy - France
Tel: 33 1 69 53 63 20 Fax: 33 1 69 30 90 79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann-Ring 125
D-81739 Muenchen, Germany
Tel: 49 89 627 144 0 Fax: 49 89 627 144 44

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleone Pas Taurus 1
Viale Colleoni 1
20041 Agrate Brianza
Milan Italy
Tel: 39 39 6899939 Fax: 39 39 689 9883

JAPAN


Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shin Yokohama
Kohoku-Ku, Yokohama
Kanagawa 222 Japan
Tel: 81 45 471 6166 Fax: 81 45 471 6122

9/3/96



MICROCHIP

All rights reserved. © 1996, Microchip Technology Incorporated, USA. 9/96

 Printed on recycled paper.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights. The Microchip logo and name are registered trademarks of Microchip Technology Inc. All rights reserved. All other trademarks mentioned herein are the property of their respective companies.